REMARKS

Claims 1-12 are pending in the application.

Claims 1, 5-9 and 11 are rejected under 35 USC § 102(e) as being anticipated by Natsume et al. (US Patent No. 6,523,138).

Natsume is directed to a system with channel processor redundancy in which channels assigned to one processor are switched to another processor when the first processor fails or indicates an error condition. Natsume does not teach a system controller operable to quiesce masters from the set of masters. The text referred to in column 9, lines 7-15 merely demonstrates that in Natsume, when a first processor fails the second processor copies a table that has the channels configured to first processor so the processor can switch the channels. There is no indication that the masters are quiesced in masters other than the one who has the error condition. Indeed, in Natsume, the master that is stopped is the one that has an error condition.

Claim 1 requires that the system controller first determine if the error message is one that determines if the quiesce is triggered. This is not shown, taught nor suggested by Natsume. In Natsume, if an error condition occurs, the processor is shut down and its channels transferred to the other processor. No quiescing of masters other than the one receiving the error condition occurs, if one were to assume that quiescing and detecting an error condition are the same, which they are not. Further, there is no error processor that processes that handles the error. The SVP in Natsume detects the error and then moves the channel control allocation and clears the error, the master that received the error does not clear the error, as is required by the invention as claimed. Therefore it is submitted that claim 1 is patentably distinguishable over the prior art and allowance of this claim is requested.

Claim 5 depends from claim 1 and should be ruled allowable for that reason and for its own merits. The text referred to at column 8, lines 66-67 and column 9, lines 1 and 2,

discuss the identification of an error condition, not that the condition is programmable. The conjunction of this with the determination of whether an error triggers quiesce is not shown, taught nor suggested by Natsume. It is therefore submitted that claim 5 is patentably distinguishable over the prior art and allowance of this claim is requested.

Claim 6 has been amended to include limitations similar to claim 1 and should be ruled allowable for the reasons as applied to claim 1. It is submitted that claim 6 is patentably distinguishable over the prior art and allowance of this claim is requested.

Claim 7 depends from claim 6 and should be ruled allowable for that reason and on its own merits. It is submitted that claim 7 is patentably distinguishable for the reasons as applied to claim 5 and allowance of this claim is requested.

Claim 8, as amended, requires that a determination be made as to whether an error triggers quiesce and then generating quiesce for selected masters. There is no indication in Natsume that there is any determination of whether an error causes the switch over or not. It appears that if the error condition occurs the channels are switched. There is no quiesce operation on selected masters as claimed in claim 8. It is submitted that claim 8 is patentably distinguishable over the prior art and allowance of this claim is requested.

Claims 9 and 11 depend from claim 8 and should be ruled allowable for that reason and for their own merits. With regard to claim 9, the selected master in Natsume is analogous to the master that had the error, while the selected masters in the instant invention are those that are not handling the error. Therefore, re-enabling the selected masters is not the same as in the invention as claimed. With regard to claim 11, as discussed above, the text in Natsume merely defines the system controller to detect errors, not to program which errors trigger the switch and which do not. It is submitted that claims 9 and 11 are patentably distinguishable over the prior art and allowance of these claims is requested.

Claim 2 is rejected under 35 USC § 103(a) as being unpatentable over Natsume et al. in view of Armany et al. (US Patent No. 6,412,027).

As discussed above with regard to claim 1, Natsume does not teach all of the limitations of amended claim 1. The addition of Armany, which sets out the function of a DMA, does not overcome the deficiency. The combination of references does not teach the limitations of the base claim, much less the limitations of the base claim in conjunction with claim 2. It is submitted that claim 2 is patentably distinguishable over the prior art and allowance of all claims is requested.

Claim 3 is rejected under 35 USC § 103(a) as being unpatentable over Natsume et al. in view of Potter (US Patent No. 5,608,884).

As discussed above with regard to claim 1, Natsume does not teach all of the limitations of amended claim 1. The addition of Potter, which sets out the function of a PCI controller, does not overcome the deficiency. The combination of references does not teach the limitations of the base claim, much less the limitations of the base claim in conjunction with claim 3. It is submitted that claim 3 is patentably distinguishable over the prior art and allowance of all claims is requested.

Claim 4 is rejected under 35 USC § 103(a) as being unpatentable over Natsume et al. in view of Holm et al. (US Publication No. 2002/0152334).

As discussed above with regard to claim 1, Natsume does not teach all of the limitations of amended claim 1. The addition of Holm, which sets out the function of a PCI bus, does not overcome the deficiency. The combination of references does not teach the limitations of the base claim, much less the limitations of the base claim in conjunction with claim 4. It is submitted that claim 4 is patentably distinguishable over the prior art and allowance of all claims is requested.

Claim 10 is rejected under 35 USC § 103(a) as being unpatentable over Natsume et al. in view of Berg et al. (US Patent No. 6,629,184).

As discussed above with regard to claim 1, Natsume does not teach all of the limitations of amended claim 8. The addition of Berg, which sets out the definition of an interrupt as an error message, does not overcome the deficiency. The combination of references does not teach the limitations of the base claim, much less the limitations of the base claim in conjunction with claim 10. It is submitted that claim 10 is patentably distinguishable over the prior art and allowance of all claims is requested.

Claim 12 is rejected under 35 USC § 103(a) as being unpatentable over Natsume et al. in view of Yazdy (US Patent No. 5,815,676).

As discussed above with regard to claim 8, Natsume does not teach all of the limitations of amended claim 8. The addition of Armany, which sets out the signaling to a bus arbiter to stop grants, does not overcome the deficiency. The combination of references does not teach the limitations of the base claim, much less the limitations of the base claim in conjunction with claim 12. It is submitted that claim 12 is patentably distinguishable over the prior art and allowance of all claims is requested.

No new matter has been added by this amendment. Allowance of all claims is requested. The Examiner is encouraged to telephone the undersigned at (503) 222-3613 if it appears that an interview would be helpful in advancing the case.

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Respecttfully submitted,
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